CSE 140L Lab 3

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# Academic Integrity

Your work will not be graded unless the signatures of all members of the group are present beneath the honor code.

To uphold academic integrity, students shall:

* Complete and submit academic work that is their own and that is an honest and fair representation of their knowledge and abilities at the time of submission.
* Know and follow the standards of CSE 140L and UCSD.

Please sign (type) your name(s) below the following statement:

I pledge to be fair to my classmates and instructors by completing all of my academic work with integrity. This means that I will respect the standards set by the instructor and institution, be responsible for the consequences of my choices, honestly represent my knowledge and abilities, and be a community member that others can trust to do the right thing even when no one is watching. I will always put learning before grades, and integrity before performance. I pledge to excel with integrity.

(NG Zhe Wee)

# Free Response

Please answer the following questions.

## Please upload a diagram of your state machine for part 1. (3 pts)

It can be a picture or digital image. Please have a state for every state in the starter code (You can find the enums starting line 17 in traffic\_light\_controller1.sv)

TODO

## Please upload a diagram of your state machine for part 2. (3 pts)

It can be a picture or digital image. Please have a state for every state in the starter code (You can find the enums starting line 24 in traffic\_light\_controller2.sv)

TODO

## How did the testbench test your implementation for part 1? (3 pts)

Word limit: 300 words

TODO

## How did the testbench test your implementation for part 2? (3 pts)

Word limit: 300 words

TODO

# Screenshots

## Part 1

### Screenshot of the RTL viewer top level schematic/block diagram in Quartus (3 pts)

TODO

### Screenshot of your waveform viewer, showing the presence of traffic and the states of the traffic signals. (3 pts)

TODO

### Please include the output file of part 1 testbench in your submission, and name it “output1.txt” (3 pts) Please submit this with code.

We will be looking for a text file with that name specifically, so be sure to rename it. Nothing is required in the writeup for this question.

## Part 2

### Screenshot of the RTL viewer top level schematic/block diagram in Quartus (3 pts)

TODO

### Screenshot of your waveform viewer, showing the presence of traffic and the states of the traffic signals. (3 pts)

TODO

### Please include the output file of part 2 testbench in your submission, and name it “output2.txt” (3 pts) Please submit this with code.

We will be looking for a text file with that name specifically, so be sure to rename it. Nothing is required in the writeup for this question.